REMARKS/ARGUMENTS

Favorable consideration of this application in light of the following discussion is respectfully requested.

Claims 1-4 are pending in this application.

In the outstanding Office Action, Claim 1 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee (U.S. Patent 5,426,447) in view of Yamazaki et al. (U.S. Patent No. 6,219,022, hereinafter Yamazaki); Claim 2 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee and Yamazaki, and further in view of Kwon (U.S. Patent No. 5,850,216); Claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee and Yamazaki, and further in view of Koyama et al. (U.S. Patent No. 6,177,920; hereinafter Koyama); and Claim 3 was indicated as allowable.

Applicants acknowledge with appreciation the indication of allowable material.

Applicants acknowledge with appreciation the personal interview between the Examiner and Applicants' representative on July 21, 2003. During the interview of July 21, 2003, the presently claimed invention was discussed in relation to Applicants' Figure 1 disclosure. As noted in the interview, Figure 1 shows an exemplary configuration of N data lines (vertical lines) divided into P blocks of N' lines (e.g., N'= 9 and lines C1-C9 comprise the first portion), and M sampling lines (e.g., horizontal lines L1 – L4). Each block receives in parallel one of the P data signals which are demultiplexed by sampling signals (DW1 – DW9), wherein the timing of the sampling signals are controlled so that for the claimed patterns of forward and backward scans are performed.[1] The Examiner indicated that in light of the explanation provided during the interview, it appeared that the combination of Lee and Yamazaki does not teach all the features of Applicants' claimed invention. However, formal

[1] Specification, page 4, line 27 – page 5, line 16.

agreement was not reached as the Examiner wished to further consider these references upon receipt of a formal response to the pending Official Action.

Briefly recapitulating, the present invention is directed to a process for displaying data on a matrix display having N data lines and P selection lines. At the intersections of these lines are image points or pixels in which the N data lines are grouped into P blocks of N' data lines (N = P x N'). Each block receives in parallel one of the P data signals which is demultiplexed on the N' lines of the block. The scanning of the N' data lines of a block is carried out from 1 to N' and from N' to 1, alternately according to the selection lines. This allows for a display without introducing a DC error of several tens of mV between the first column sampled in the block and the last, as is common in conventional systems.[2]

Lee discloses a method for demultiplexing Y data selection signals over X groups of Y data lines. In particular, Lee discloses pixels located at the intersection of data lines and row lines.[3] In Lee, the number of data lines is equal to the number of groups multiplied by the number of data lines/group.[4] As noted in the Office Action,[5] Lee does not disclose alternately scanning of the N' data lines of a block from 1 to N' and from N' to 1 according to the selection lines as recited in Applicants' Claim 1.

Yamazaki discloses an electro-optical liquid crystal display device comprising a plurality of display portions where each display portion may display data separately from another display portion.[6] However, contrary to the Official Action,[7] Figure 15 of Yamazaki does not teach or suggest alternately scanning of the N' data lines of a block from 1 to N' and from N' to 1 according to the selection lines, as recited in Applicants' Claim 1. Instead Figure 15 of Yamazaki teaches repeated scanning a display portion in a first direction

[2] Specification, page 3, lines 11-21.
[3] Lee, column 5, lines 31-37 and column 6, lines 33-41.
[4] Lee, column 6, lines 48-60.
[5] Office Action, page 6, lines 3-4.
[6] Yamazaki, column 7, lines 18-24.
[7] Official Action, page 3, lines 8-11.

followed by resetting the scan to the first column. In Figure 9, Yamazaki teaches a plurality of blocks, some of which are scanned in one direction and others of which are scanned in directions orthogonal to the first direction. However, Yamazaki does not teach or suggest Applicants' claimed feature of 'each block receiving in parallel one of the P data signals which is demultiplexed on the N' lines of said block, wherein, alternately, according to the selection lines, the scanning of the N' data lines *of a block* is carried out from 1 to N' and from N' to 1.' In Yamazaki, the scanning *within a block* is performed by scanning a line in a first direction, resetting the scan, and then scanning the next line in the *same direction* as the first direction. Thus, Applicants submit that Yamazaki is another example of the conventional art described in Applicants' invention.[8]

Applicants have also considered Kwon and Koyama and submit that neither of these references cure the deficiencies of Lee and Yamazaki. Kwon teaches changing a scanning direction of a single line based on a scanning signal DWN.[9] Koyama teaches a synchronous clock signal to change a scanning direction of a single line.[10] Neither Kwon nor Koyama teach or suggest alternately scanning of the N' data lines of a block from 1 to N' and from N' to 1 according to the selection lines, as recited in Applicants' Claim 1. Applicants therefore traverse the outstanding rejection of Claim 1 as none of the cited prior art, individually or in combination, disclose or suggest all the elements of independent Claim 1. Therefore, Applicants submit the inventions defined by Claim 1, and all claims depending therefrom, are not rendered obvious by the asserted prior art for at least the reasons stated above.[11]

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[8] Specification, page 3, lines 2-17.
[9] Kwon, column 10, lines 64-67.
[10] Koyama, column 8, lines 27-44.
[11] MPEP § 2142 "...the prior art reference (or references when combined) must teach or suggest **all** the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)."

Furthermore, Applicants submit there is no teaching, suggestion, or motivation, either explicitly or implicitly, in either reference to combine the unidirectional demultiplexer circuit 102 of Lee with the orthogonal unidirectional scan technique of Yamazaki to arrive at Applicants' inventions recited in Claim 1. That is, neither reference mentions DC errors associated with the order of sampling data signals *within a block*. Thus, Applicants submit it is only through an impermissible hindsight reconstruction of Applicants' invention that the rejection of Claim 1 can be understood.[12]

Accordingly, in light of the previous discussion, Applicants respectfully submit that the present application is in condition for allowance and respectfully request an early and favorable action to that effect.

Respectfully submitted,

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[12] MPEP § 2143.01 "Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge of one of ordinary skill in the art."